SPECIFICATION

Please amend the paragraph bridging pages 4-5 as follows:

Consequently, several other delay metrics based on higher-order moments have been proposed, see e.g., A. B. Kahng and S. Muddu, "Two-pole Analysis of Interconnection trees," Proceedings IEEE Multi-Chip Module Conference, Santa Cruz, February 1995, pp. 105-110 and A. B. Kahng and S. Muddu, "A General Methodology for Responses and Delay Computations in [[VSLI]] VLSI Interconnects," UCLA CS Dept. TR-940015, 1994. While these approaches are typically more accurate than Elmore and simpler than truly accurate methods, see e.g., L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis," IEEE TCAD, 9(4), 352-366, 1990, some of the simplicity of the Elmore delay is lost. All of these metrics use multiple moments of the transfer function, which makes them non-additive.

Please amend the paragraph beginning at page 6, line 10 as follows:

To achieve the foregoing objects, and in accordance with the invention as embodied and broadly described herein, a method for determining an interconnect delay at a node in an interconnect having a plurality of nodes is disclosed. The method includes performing a bottom-up tree traversal to compute the first three admittance moments for each of the nodes in the interconnect. The computed admittance moments are utilized, in an advantageous embodiment, to compute a pi-model of the downstream load. Next, the equivalent effective capacitance value C_{eff} is computed utilizing the components of the computed pi-model and the Elmore delay at the node under evaluation. In an advantageous embodiment, C_{eff} is characterized by:

$$C_{eff} = C_{fj}(1 - e^{-T/\tau dj})$$

where C_{fj} is the far-end capacitance of the pi-model at the node, T is the Elmore delay at the node and τdj is the resistance of the pi-model (R_{dj}) multiplied by C_{fi} [[C_{fi}]]. The interconnect delay at the node (ECM_j) is then determined utilizing an effective capacitance metric (ECM) delay model characterized by:

$$ECM_j = ECM_{p(j)} + R_j(C_j + C_{xj} + C_{eff})$$

where $ECM_{p(j)}$ is the computed ECM delay at the node immediately preceding the node under evaluation, R_j is the resistance between the node under evaluation and the preceding node, C_j is the capacitance to ground at the node under evaluation and C_{xj} is the near-end capacitance of the pi-model at the node under evaluation.

Please amend the paragraph beginning at page 11, line 1 as follows:

Assume a RC tree with nodes $\{v_o, ..., v_N\}$ where v_o is the source. Let C_i be the capacitance at node v_i [[v_1]] for $0< i \leq N$, and let R_{ki} be the total resistance of the portion of the unique path from v_o to v_i that overlaps with the unique path from v_o to v_k. The Elmore delay to node v_i is given by the formula:

$$ED_i = \sum_{k=1}^{N} R_{ki}C_k \qquad (3)$$

From the formula, one can see that two tree traversals are sufficient to compute the Elmore delay.

Please amend the paragraph beginning at page 11, line 27 as follows:

Tutuianu et al., "Explicit RC-Circuit Delay Approximation Based on the First Three Moments of the Impulse Response," IEEE/ACM DAC, 1996, pp. 611-616, teaches a closed-form approximation for estimating delay for step inputs. More recently, Kay and Pileggi, "PRIMO: Probability Interpretation of Moments for Delay Calculations," IEEE/ACM design Automation Conference, 1998, pp. 463-468, proposed PRIMO that fits the moments of the impulse response to probability density functions. First, the parameters to the probability density function must be computed from the moments, and then a single table lookup operation is all that is required to produce the delay. Lin et al., "h-gamma: An RC Delay Metric Based on a Gamma Distribution Approximation to the Homogeneous Response," IEEE/ACM ICCAD, pp. 19-25, improved upon PRIMO with the h-gamma metric. H-gamma ~~h-gamma~~ avoids time-shifting the distribution functions and matching moments to the circuit's [[homogenous]] homogeneous response. However, for fast evaluation, a 2-D table needs to be carefully constructed.

Please amend the paragraph bridging pages 14-15 as follows:

The ECM delay model of the present invention, instead of modeling the downstream capacitance by a single value C_{dj}, represents the downstream capacitances from node j under evaluation with an equivalent effective capacitance, determined utilizing a pi-model as depicted in FIGURE 1B, to capture resistive shielding. It should be readily apparent to those skilled in the art that the determination of the equivalent effective capacitance is not limited to one particular modeling scheme, in other embodiments, a tee-model may also be advantageously utilized. To compute the pi-model, the input admittance Y(s) of the circuit downstream of j is expanded in a Taylor series about s = 0 as follows:

$$Y_j(s) = y_1 s + y_2 s^2 + y_3 s^3 + ... \quad (6)$$

where y_1, y_2, ..., etc., are the moments of the admittance for node j. Note that the dc component y_0 is zero since it has been assumed that there is no dc path to ground. The three components of the pi-model, i.e., R_{dj}, C_{fj} and C_{nj}, are given by:

$$R_{dj} = [[-y^2_{3j}/y^3_{2j}]] = (y_{3j})^2/(y_{2j})^3,$$
$$C_{fj} = y^2_{2j}/y_{3j}, \text{ and}$$
$$C_{nj} = y_{1j} - C_{fj}.$$

Please amend the paragraph beginning at page 15, line 4 as follows:

For a detailed example for computing the components of the pi-model, see P. R. O'Brien, et al., "Modeling the Driving point Characteristic of Resistive Interconnect for Accurate Delay Estimation," IEEE/ACM ICCAD, 1989, pp. 512-515, which is herein incorporated in its entirety by reference. Following the determination of the components of the pi-model that captures the downstream load, the single RC circuit of resistance R_{dj} and C_{fj} (illustrated in FIGURE 1B) is modeled by a single effective capacitance C_{eff} (where $C_{eff} < C_{fj}$) as depicted in FIGURE 1C. The ECM delay model of the present invention is thus given by:

$$ECM_j = ECM_{p(j)} + R_j(C_j + C_{nj} + C_{eff}) \quad (7)$$

where

$$C_{eff} = C_{fj}(1 - e^{-T/\tau dj}) = C_{fj}(k) \quad (8)$$

Please amend the paragraph beginning at page 16, line 26 as follows:

Data processing system 200 also includes a random access memory (RAM) 220, read only memory (ROM) [[210]] 215 and input/output (I/O) adapter 225 for connecting peripheral devices, such as disk units 230 and tape units 235 to system bus 250. A user interface adapter 260 is utilized to connect a keyboard device 255 and a mouse (not shown) to system bus 250 while a display adapter 265 couples a display device 270, such as a monitor, to system bus 250. A communication adapter 240 is also depicted for coupling data processing system 200 to an external network, generally designated 275.